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# 1<sup>st</sup> HONORARY MENTION

## Low Power In-Memory Implementation of Ternary Neural Networks with Resistive RAM-Based Synapse

A. Laborieux, M. Bocquet, T. Hirtzlin, J.-O. Klein, L. Herrera Diez, E. Nowak, E. Vianello, J.-M. Portal, and D. Querlioz

Univ. Paris-Saclay, CNRS; IM2NP Univ. Aix-Marseille, CNRS; CEA-LETI, Grenoble - France

A blue ink signature of Bernabe Linares-Barranco.

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A blue ink signature of Youngsu Kwon.

Youngsu Kwon  
Best Paper Award Co-Chair

